UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,171	12/22/2003	Karl H. Jacobs	TI-36859 (UNITI-173XX)	7745

7590 05/06/2005

W. Daniel Swayze, Jr. Esq.
Texas Instruments Incorporated
M/S 3999
P.O. Box 655474
Dallas, TX 75265

EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/743,171	JACOBS ET AL.	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,10,11,19-21,26 and 31* is/are rejected.

7)☒ Claim(s) *3-6,8,9,12-18,22-25,27-30,32-37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's Amendment filed on 4-6-05 has been received and entered in the case. The rejections set forth in the previous Office Action are maintained as indicated below.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 7, 10-11, 19-21, 26 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by the Petted et al reference (U.S. Patent 5,153,469).

Petted discloses in figures 2 and 3 an apparatus comprising an input voltage node (input of 30); an output voltage node (common node of W1 and W2) coupleable to a load (W1); a first circuit node (at gate of W2); a first transistor W2 having gate, source, and a drain, the drain of the first transistor being coupled to the output voltage node, source of first transistor being coupleable to a first voltage source (GND), wherein the first transistor biased to operate within its active operating region; feedback resistor 52 having first and second terminals coupled to the output voltage node and the first circuit node, respectively, the feedback resistor being connected between the gate and the drain first transistor; and an input resistor (30) having first and second terminals coupled to the second terminal of the feedback resistor and the input voltage node, respectively, as required by claim 1. It is noted that the limitation "wherein the control circuit is operative to provide ramped down voltage signal at the output voltage node that linearly tracks a

first ramped voltage signal applied to the input voltage node" is seen as a result derived from the above apparatus.

As to claim 2, col. 3, lines 20-25, indicates that transistor W2 can be either NMOS or PMOS.

As to claim 7, circuit 10 in figure2 is seen as a level shifting circuit coupled between the second terminal of the input resistor 30 and input voltage node.

As to claim 10, resistor 54 is seen as a bias current source coupled to the gate of the first transistor. Further, it is inherent that the bias current source being operative to bias the first transistor within its active operating region.

As to claim 11, the scope of claim is similar to that of claim 10. Therefore, it is rejected for the same reason set forth above.

As to claims 19-21, 26 and 31, they are rejected for reciting a method/step derived from apparatus described in claims 1, 2, 7, and 10-11 as noted above.

Response to Arguments

3. Applicant's arguments filed 4-6-05 have been fully considered but they are not persuasive.

Applicant argues that "*Petted does not disclose or suggest the presently claimed invention including the control circuit being operative to provide a ramped down voltage signal at the output voltage node that linearly tracks a first ramp up voltage signal applied to the input voltage node in independent claim 1*".

Examiner respectfully disagrees with Applicant's position for the following reasons:

a. As voltage increases at the input (i.e., ramp up the gate of transistor), transistor 42 gradually turns on (i.e., conducting) to pull the output node down to Ground (i.e., ramp down voltage signal at the output voltage node). In other words, Petted's circuit suggests the limitation *a ramped down voltage signal at the output voltage node linearly tracks a first ramp up voltage signal applied to the input voltage node.*

b. Petted discloses each and every component required by the recitation of claim 1, including their configuration relationships. Therefore, the operation of Petted's circuit must be the same as that of required by claim 1. If Applicant believes that his circuit operates different from that of Petted's invention, then there must be some other limitation and/or component, which are not recited in the claim of the instant application. .

In addition, Applicant alleges that *"[T]he Examiner acknowledges that Petted does not disclose this feature*" (the above argument). Examiner respectfully disagrees since there is no such a statement in the Office Action dated 01-10-05.

Lastly, Applicant concludes that *"[T]he combination of circuit and control circuit of the present invention*" brings about the advantageous result. Examiner respectfully disagrees since there is no such combination as recited in claim 1 of the instant application. Claim 1 calls for a slew rate control circuit comprising in/output nodes, a transistor and two resistors wherein the limitation "*the control circuit*", line 19, refers "*a slew rate control circuit*" recited on line 1 of claim. Thus, there is no combination of circuit and the control circuit as alleged by Applicant.

Allowable Subject Matter

4. Claims 3-6, 8, 9, 12-18, 22-25, 27-30 and 32-37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose an apparatus and method thereof comprising elements being configured as recited in claims. Specifically, none of the prior art teaches or fairly suggests, among other things, the following limitations:

- The ramped down voltage signal provided at the output voltage node ramps down from 0 volts to a first negative voltage level as required by claims 3 and 22.
- The level shifting circuitry is operative to level shift a second ramped up voltage signal applied to the input voltage node to the first ramped up voltage signal provided at the second terminal of the input resistor as required by claims 8 and 27.
- The controlled bias current source coupled to the gate of the first transistor, the controlled bias current source being operative to bias the first transistor within its active operating region by applying a controlled current to the gate of the first transistor as required by claims 12 and 32.
- The controlled bias current source is operative to apply the controlled current to the gate of the first transistor after the first ramped up voltage signal ramps to a predetermined voltage level and after a predetermined time delay, thereby reducing

an on-resistance between the drain and the source of the first transistor as required by claims 14 and 34.

- A third resistor coupled between the first circuit node and the gate of the first transistor, wherein a voltage across the third resistor is operative to provide compensation for a voltage across the gate and the source of the first transistor as required by claims 18 and 29.
- The controlled bias current source is operative to sequentially increase a level of the controlled current applied to the first transistor gate from a first current level to at least one second current level greater than the first current level after the first ramped up voltage signal ramps to a predetermined voltage level as required by claims 16 and 36. And,
- A combination of the first transistor and the feedback resistor forms a closed control loop, and further including a controllable switch disposed within the control loop, the switch being controllable to open before the controlled current is applied to the gate of the first transistor' by the controlled bias current source as required by claims 17 and 37.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
4-20-05 ATL

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800